

## REMARKS

Claims 1-11 are pending in the present application. With this Response, Applicants amend claim 1. Support for this amendment may be found, for example, at page 7, line 4 through page 9, line 20 of Applicants' specification. No new matter is introduced.

### REJECTION UNDER 35 U.S.C. § 103

Claims 1, 2 – 8 and 11 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,016,317 to Sakurai et al. in view of U.S. Patent No. 6,185,209 to Wicklund. Claims 9 and 10 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sakurai in view of U.S. Patent No. 5,535,197 to Cotton. Applicants amend claim 1 to further clarify the nature of their invention, and respectfully traverse the rejections.

In a Response of November 21, 2003, Applicants made the following arguments:

In amended independent claim 1, Applicants disclose a common buffer memory control apparatus for storing ATM message data items, comprising a first management means for tracking free and used blocks in the common buffer memory, block selecting means for selecting a free block based on information provided by the first management means for storing a single message data item, cell writing control means for controlling the writing of the single message data item so that the cells are written in the selected block, and single message extracting means for extracting the respective cells written in the selected block by the cell writing control means as a single data message item when a cell at the tail of the single message data item is received.

Sakurai discloses an ATM cell switching system for multiplexing and outputting cell trains. As depicted in FIG. 2 of Sakurai, the system of Sakurai is similar to the system disclosed by Applicants in their FIG. 1 depiction of the prior art (AAPA). Consistent with Applicants' description in association with AAPA (see, e.g., Applicants' specification at page 2, lines 21 through page 3, line 34), the system of Sakurai causes cells associated with a single message to be stored in a queue chain in a common buffer nearby such that reading of a single message from the common buffer memory requires a successive address read for each cell read (see, e.g., column 5, line 52 through column 6, line 25 of Sakurai).

The Examiner acknowledges that Sakurai fails to disclose Applicants' single message extracting means, but asserts that the missing limitation is taught by Wicklund.

Wicklund discloses an ATM switching device 110 having a switch core 112 directing cells to a plurality of pre-merge queues 140 and merge queues 144 for packaging cells into packets (see, e.g., FIG. 2 of Wicklund). As illustrated by FIG. 3A of Wicklund, a current cell in an ATM message is linked to a previous cell in the ATM message in order to effectively enable reading of a the collection of cells as a single message. However, in sharp distinction to Applicant's apparatus of amended claim 1, both Sakurai and Wicklund collectively and individually fail to teach or suggest Applicant's claim limitation requiring that the single data message item be accumulated and written to one selected block. Applicant's claimed apparatus thereby provides a significant advantage over Wicklund in eliminating the need for cell pointers to identify all cells associated with a single message, thereby avoiding pointer bit allocations, coding steps and other associated overheads.

The Examiner finds this argument to be unpersuasive, suggesting that the argued limitation ("single data message item be accumulated and written to one selected block") is not recited in the rejected claim. Applicants amend claim 1 to clearly recite "cell writing control means for controlling a write operation for the single message data item so that the respective cells of the single message data item are accumulated in the one block, selected by said block selecting means" (see, e.g., page 8, lines 11 – 32 of Applicants' specification).

The Examiner further suggests that FIG. 2 of Sakurai discloses received cells multiplexed by multiplexer 12 before being input to buffer memory 11, and argues that by retrieving the tail of the last cell written to locate the next free location, multiplexed cells are stored contiguously in buffer memory 11.

Sakurai discloses a system in which cells associated with a single message are progressively stored in a queue chain, where a next address is selected from idle address buffer 103 (see, e.g., column 5, lines 61 – 65 of Sakurai) and stored in a common buffer nearby. As a result, a single message from the common buffer memory requires a successive address read for each cell read.

Sakurai provides no clear means for cells associated with a single message to receive successive addresses that contiguous and within a single memory block. In other words, Sakurai fails to disclose Applicants' claimed block selecting means for selecting one full block of free memory to which the cells of the single message will be written, and single message extracting means for extracting cells of s single message as the single message data from the one block when a cell at a tail of the single message data item is received.

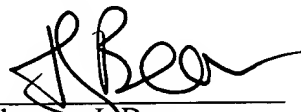
Accordingly, Applicants submit that independent claim 1 is not made obvious by Sakurai and Wicklund, either alone or in combination, and is therefore in condition for allowance. As dependent claims 2 – 11 depend either directly or indirectly from allowable claim 1, Applicants further submit that claims 2 – 11 are allowable for at least this reason.

#### CONCLUSION

In view of the amendments and set forth above, this application is in condition for allowance which action is respectfully requested. However, if for any reason the Examiner should consider this application not to be in condition for allowance, the Examiner is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper may be charged to Deposit Account No. 50-1290.

Respectfully submitted,



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